Amendments to the Specification

Please replace the paragraph beginning on page 15, line 16, with the following rewritten paragraph.

As shown in Fig. 3, adjustable pulse delay 16 may, in some embodiments, include plurality of delay cells 33_0–33_n. Each delay cell may include gate 34, delay block 35 and multiplexor 36 as depicted in delay cell 33_0. In addition, adjustable pulse delay 16 may include baseline delay 37. As shown in Fig. 3, adjustable pulse delay 16 may be configured to send signals from baseline delay 37 to multiplexor 36 of delay cell 33_0. In addition, adjustable pulse delay 16 may be configured to send an output signal from a multiplexor of one delay to the multiplexor of the succeeding delay. In this manner, the delay of a signal transmitted through the circuit may be determined by summing the delays through which the signal traverses. In general, delay block 35 may include any number of delay units within each of delay cells 33_0–33_n. In some embodiments, the number of delay units within each delay block may correspond to the position of its corresponding delay cell within plurality of delay cells 33_0–33_n, as shown in Fig. 3. In particular, the delay blocks within delay cells 33_0–33_n may, in some embodiments, include 2^n units. In other embodiments, the number of delay units within each delay block may not correspond to the position of ~~it~~ the corresponding delay ~~cell~~ cells within delay cells 33_0–33_n.

Please replace the paragraph beginning on page 30, line 21 with the following rewritten paragraph.

Such a system failure may be prevented, however, by including a circuit within MRAM device 10 that is configured to terminate applications of current along bit and/or digit lines before the magnetization states of one or more magnetic elements selected for a write operation of the device are changed. For example, MRAM device 10 may include write protect 28 as shown in Fig. 1. An exemplary circuit for write protect 28 is illustrated in Fig. 11 and described in more detail below. Other circuitry may be used for write protect 28, however, depending on the design specifications of MRAM device 10. In particular, write protect 28 may include any

circuitry which is configured to monitor a power supply voltage to MRAM device 10 and terminate applications of current along bit and/or digit lines of magnetic memory arrays 12 upon determining the power supply voltage is below ~~than a~~ predetermined threshold.